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# Characterization of the GaP/Si(001) interface by transmission electron microscopy

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ABSTRACT: A Transmission Electron Microscopy study of ALMBE grown GaP/Si(001) is presented. A high density of microtwins, stacking faults and threading dislocations is observed in the epilayer. The lattice mismatch at the GaP/Si interface appears not to be relaxed by edge or 60° dislocations but primarily by planar defects. Post-thermal annealing treatments are shown to drastically diminish the density of microtwins and stacking faults, and slightly decrease the threading dislocation density.

## INTRODUCTION

The possibility of growing III-V semiconductor compounds on Si (001) has attracted great interest in the last few years due to the low cost of the substrate and to the inherent advantages of integrating III-V devices into Si technology. To date, a large number of III-V semiconductor compounds have been grown on Si (001) by different epitaxial growth techniques (e.g. MBE, MOCVD, CBE). However, the high lattice mismatch and the difference in the thermal expansion coefficient that exist between the III-V semiconductors and Si tend to generate a high density of defects in the epilayers. The GaP on Si system (lattice mismatch = 0.36%) was one of the first where it was demonstrated that III-V semiconductors could be successfully grown on Si (Pirouz et al 1988). However, the defect density and morphology were similar to those observed in systems with a much larger lattice mismatch. This problem was associated with the particular growth mechanism involved. Several authors have studied the microstructural quality of the GaP/Si (001) system grown by different growth techniques e.g. MOCVD (Olson et al 1987), LPMOCVD (Soga et al 1988). In this paper a TEM study of the GaP/Si (001) system fabricated by Atomic Layer Beam Epitaxy (ALMBE) is presented

## EXPERIMENTAL

The ALMBE method is an alternative epitaxial growth technique based on a continuous supply of group III flux and periodic short pulses of group V flux (Ruiz et al 1989). Two samples consisting of 1 μm thick GaP epilayers were deposited on (001) silicon substrates tilted 2° off toward [110] at a growth temperature of 350°C. Sample A was given two thermal cycles to 580°C partway through growth. Sample B was grown under identical conditions, but was given an additional 580°C heat treatment for 10 minutes after the growth was completed. Plan-view TEM specimens were prepared by chemical etching methods and the cross-sectional specimens by Ar ion milling after mechanical thinning. Electron Microscopy studies were performed on a

JEOL 1200-EX and a JEOL 2000-EX operating at 120 kV and 200 kV, respectively.

## RESULTS AND DISCUSSION

Sample A was found to have a defect morphology similar to that reported previously for the GaP/Si(001) system grown by other techniques. A high defect density originated at the GaP/Si interface consisting mainly of microtwins, stacking faults and threading dislocations as shown in figures 1 and 2. The defect density in the epilayer decreases considerably with increasing distance from the interface with most of the microtwins terminating at a distance of about 70 nm from the interface.

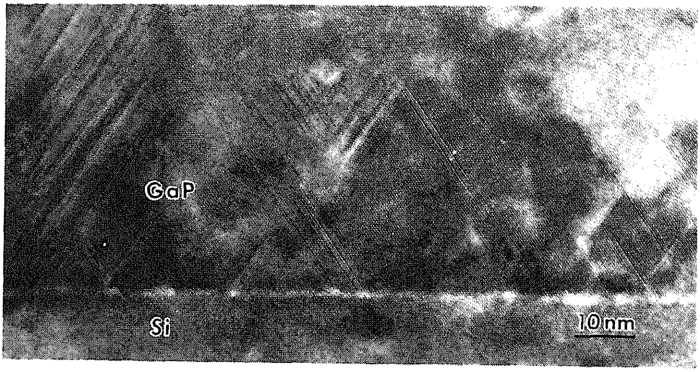

**Figure 1.** Axial [110] HREM micrograph of the GaP/Si interface in sample A.

Ernst et al (1988) have proposed that numerous microtwins and stacking faults in the GaP/Si (001) system develop as a consequence of facetted 3D island formation during the initial growth stage. The low faulting energy on {111} planes in III-V semiconductors allows planar defect formation by growth accidents on these exposed {111} facet planes. According to several authors (Olson et al 1986, Blakeslee et al 1987), residual $SiO_2$ or/and SiC at the GaP/Si interface can act as additional nucleation sites for these defects. Evidence supporting this may be seen in HREM image (figure 1), where bright patches at the interface are associated with the nucleation points of some planar defects. In a recent HREM study of GaAs/Si grown by ALMBE, Vilá et al (1993) have observed that the growth occurs coherently up to a critical layer thickness, which is different for each island depending on the height-width ratio, at which point partial dislocations appear. These dislocations subsequently react originating perfect dislocations and their associated planar defects disappear. A similar process may be occuring in our samples in which the last recombination step does not occur and the planar defects remain up to the end of the growth. Contrary to what have been seen in GaP/Si grown by MOCVD (Pirouz et al 1988), the planar defect density in sample A is considerably higher than that for both the GaAs/Si and GaAsP/Si systems grown by ALMBE (Molina 1993) which have a higher lattice mismatch. We believe that this is a natural consequence of the very high island nucleation density and their smaller island size at coalescence.

A detailed analysis of many cross-sectional HREM images of sample A showed no evidence of 90° or 60° dislocations present at the GaP/Si interface. In the case of total strain relaxation through misfit dislocations, a mean-separation of 1070 Å is expected for 90° dislocations in the GaP/Si system. Almost complete relaxation has occurred in sample A via the presence of planar defects. A microtwin needs to be six (111) layers thick in order to be able to accommodate the mismatch along <110> directions as efficiently as an edge misfit dislocation (Pirouz et al 1987). According to Lee et al (1991), although this type of defect relieves less stress, they are more convenient for starting relaxation because their activation requires a smaller energy.

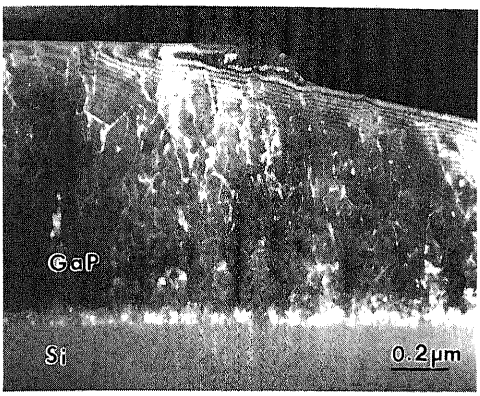

**Figure 2.** A (g=220) WB image of the GaP epilayer in sample A

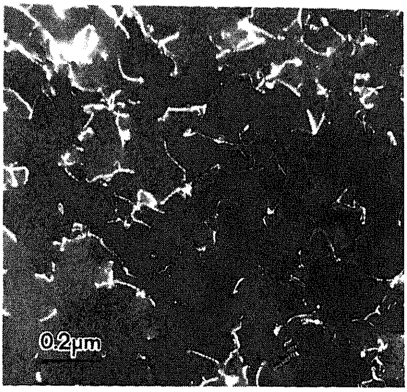

**Figure 3.** Plan-view (g=400) WB image showing the threading dislocation density near the epilayer surface in sample A.

On the other hand, a high density of threading dislocations (~$10^{10}$cm$^{-2}$) in the epilayer is evidenced in figure 3. After a systematic **gb∧u** defect analysis we found mainly partial dislocations present although some isolated edge and 60° dislocations were also found. The existence of the perfect dislocations is most likely a consequence of various reactions occurring between partial dislocations associated with the planar defects.

When a polar zincblende semiconductor is grown on a non-polar diamond cubic structure, antiphase domains often occur. However, after studying several cross-sectional specimens using the Taftφ and Spence (1982) CBED technique and applying the Nomarski technique on chemically etched plan view layers (Morizane 1977), we could not find any evidence of APBs. This could be due to the vicinal substrate.

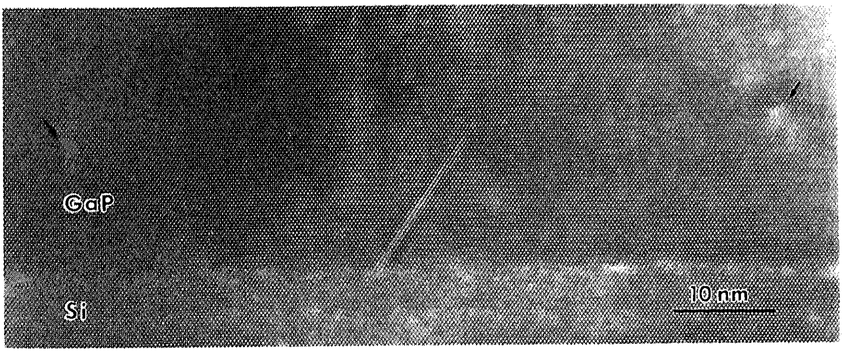

**Figure 4.** Axial [110] HREM micrograph of the GaP/Si interface in sample B.

Because of its lower growth temperature, strain relaxation in ALMBE grown samples proceeds by different routes than in the traditional high temperature techniques and metastable defects can still persist up to the end of the growth. The effect of post thermal annealing is therefore of great importance since it allows the system to reach a strain equilibrium condition. Analysis of sample B shows that the final thermal annealing step changes the defect density and morphology considerably. The threading dislocation density in the epilayer is still high ($\sim 10^9 cm^{-2}$) and dislocation loops with diameters smaller than 80 nm have appeared (figure 5). The main effect on the microstructure however is the dramatic reduction of the planar defect density near the interface as shown in figure 4. In addition, edge dislocations appear periodically, which "stand off" about 50 Å from the interface. This dislocation configuration may be attributable to planar defect recombination during the thermal annealing and is currently under further investigations.

**Figure 5**. Plan-view (g=400) WB image showing the threading defects and dislocation loops near the epilayer surface in sample B.

## CONCLUSIONS

In summary, our TEM observations of GaP layers grown on Si (001) by ALMBE suggest that the 3D island growth mechanism results in considerable planar defect formation. The planar defect density is in fact higher than for GaAs/Si (001) system which has a much larger lattice misfit. The strain relaxation appears to occur mainly via these planar defects. When a post-thermal annealing treatment is curried out the planar defect density decreases dramatically with a corresponding improvement in crystalline quality. In addition series of edge dislocations which stand-off from the interface are formed to relieve misfit strain.

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