SURFACE AND INTERFACE ANALYSIS
Surf. Interface Anal. 2004; **36**: 969–972

SIA

SIMS investigation of the influence of Ge pre-deposition on the interface quality between SiC and Si

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Received 28 July 2003; Revised 27 November 2003; Accepted 27 November 2003

SiC/Si(111) heterostructures formed by using an alternative method for stress relaxation were investigated by SIMS and AES. The applied stress reduction method is based on a theoretical approach, which predicts an improvement of the SiC layer quality if Group IV elements are incorporated into the interface between SiC and Si. Germanium was chosen to test this approach. The incorporation of Ge into the heterointerface was carried out by depositing different amounts of Ge prior to the SiC growth process and varying the Ge deposition temperature. SIMS investigations revealed that Ge remains near the SiC/Si interface independently of the pre-deposited amount of Ge. In the case of two monolayers (ML) Ge coverage (with respect to the silicon surface) a surface segregation was observed. This indicates a limited transport of Ge to the SiC surface through the growing SiC layer due to grain boundary diffusion. At Ge coverages between 0.5 ML and 2 ML a sharper interface between the SiC and Si was observed. In this case the tail of the carbon distribution remains within the region occupied by the Ge distribution. The incorporation of Ge at the interface suppresses the out-diffusion of Si from the substrate to the surface of the growing SiC layer and, therefore, impedes the formation of voids at the SiC/Si interface. Copyright © 2004 John Wiley & Sons, Ltd.

KEYWORDS: SIMS; AES; ellipsometry; SiC; heteroepitaxy; interface control

INTRODUCTION

The silicon carbide–silicon heteroepitaxial system has different applications in sensors, optoelectronics, electronics and as a pseudosubstrate for wide band gap semiconductors epitaxy. Owing to high lattice and thermal mismatch between SiC and Si a high residual stress and large lattice defect density exist in the grown SiC layers. Another critical issue is the silicon out-diffusion through the growing SiC layer leading to void formation at the SiC/Si interface. These phenomena lead to insufficient electrical properties of the grown SiC layer and the heterojunction. The following techniques can be used to attenuate these difficulties: (1) reduction of the growth temperature by using high reactive species and/or atomic layer epitaxy, (2) SiC growth on silicon on insulator (SOI) substrates, (3) wafer bonding, (4) SiC growth on porous or nanostructured Si, and (5) growth of SiC on Si substrates modified with Ge and N. Only the last method is applicable if the electrical properties of the heterojunction are of interest. In this paper we report on the behaviour of the pre-deposited Ge at the SiC/Si interface and the impact of this modification on the SiC/Si heterostructure grown on Si(111).

EXPERIMENTAL

The SiC layers were grown by solid source molecular beam epitaxy (SSMBE) on on-axis boron-doped p-type Si(111) substrates. The wafers had a resistivity of 1 to 10 Ω·cm. The 120 nm thick SiC layers were grown on Si in a UMS 500 Balzers MBE system. The growth procedure consists of the following process steps: (1) hydrogen plasma cleaning of the silicon substrates, (2) annealing at 750 °C for 1 h in the deposition chamber, (3) 0 to 2 ML Ge deposition on the (7×7)-Si reconstructed Si surface at 325 °C by electron beam evaporation (ML with respect to the Si(111) surface) (series 1) or deposition of 1 ML Ge at different substrate temperature ranging from room temperature to 660 °C (series 2), (4) deposition of C at 325 °C, (5) gradual increase of the substrate temperature in steps of 50 °C up to the final growth temperature for SiC epitaxy, and (6) the SiC deposition started at 850 °C with a growth rate of 1 nm/min under Si rich conditions and continuously operating Si and C sources. The epitaxial growth was carried out at 1000 °C. The stability of the deposition condition was

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controlled by monitoring the appearance/disappearance of the 3-dimensional Si nucleation and/or the intensity of (3 × 3)-Si related surface reconstruction streaks on the 3C–SiC(111) surface with *in situ* reflection high-energy electron diffraction. Additionally, the growth process was controlled by *in situ* real-time spectroscopic ellipsometry (SE) to examine the SiC thickness and the evolution of the surface and interface of the growing 3C–SiC layer. Depth profiling by SIMS was carried out with an IMS 4F Cameca. An O_2^+ primary beam with an impact energy of 14.96 kV was used. The incidence angle was 60°. AES depth profiling was carried out by using a Riber ASC 2000 machine and an Ar^+ beam with an energy of 1 keV at an angle of incidence of 60°. Further *ex situ* investigations of the epitaxial layers were carried out by atomic force microscopy and transmission electron microscopy (TEM). The thickness of the SiC layer was determined with SE by using a four-layer model.

RESULTS AND DISCUSSION

The AES measurements were not able to detect Ge in the grown SiC/Si heterostructure. This observation was in contrast to previously achieved results where Ge could be detected in the near-interface region by AES and XPS after Ge pre-deposition and subsequent carbonization under MBE conditions.[1] The obtained result indicates a Ge content below 1% at the SiC/Si interface and in the SiC layer.

The SIMS measurements revealed three types of depth profiles. They are shown in Figs 1 to 3. The *x*-axis scale was calibrated by assuming the SiC thickness in correspondence with 50% of the Si signal variation. The differences in the sputter coefficients between SiC and Si were taken into account, in agreement with Ref. 2. The SiC thickness was determined by *in situ* SE at room temperature and fitting the obtained ellipsometric data with a four-layer model (roughness: SiC and air)/(SiC)/(Si and air)/(Si). The used multilayer model was verified by transmission electron microscopy investigations.[3] The obtained depth profiles (Figs 1 to 3) can be divided into three regions: (1) the SiC layer, (2) the interface layer defined by using the silicon signal variation (84%–16%) and (3) the silicon substrate.

The most striking feature was the detection of the Ge near the SiC/Si interface at the silicon side of the heterostructure (Figs 1 to 3). The amount of the detected Ge increases with increasing Ge pre-deposition indicating a strong confinement near the SiC/Si interface and a minor contribution of Ge out-diffusion. The Ge distribution starts in the interface region. The main part of Ge is situated in the silicon substrate near the SiC/Si interface. With increasing Ge coverage prior to the Si conversion and the SiC growth the Ge distribution shifts slightly into the SiC layer, i.e. moves towards the surface. Additionally, a Ge surface segregation could be detected only at low and high Ge coverage (Fig. 4). This observation was confirmed by the SIMS measurements carried out on SiC/Si heterostructures grown on Si substrates with 1 ML Ge pre-deposited at different substrate temperatures prior to the carbonization. In this case Ge surface segregation was not observed. Moreover, the detected amount of Ge at the interface was independent of the pre-deposition temperature. The full width at half maximum (FWHM) of the Ge distribution displayed in Fig. 4 exhibits a minimum around 0.75 ML Ge. For the second series of experiments (the temperature dependence and 1 ML Ge) a minimum between 325 °C and 500 °C can be deduced (Fig. 5).

The carbon distributions show two different behaviours. The first type is shown in Figs 1 and 3 where in the near-interface region a steep decrease of the carbon concentration occurs. In larger depths a deep-reaching tail was observed. This type of carbon distribution was also observed in the case of SiC layers grown on Si(111) substrates without Ge pre-deposition, for Ge coverages deposited prior to the carbonization process and SiC growth lower than 0.75 ML,

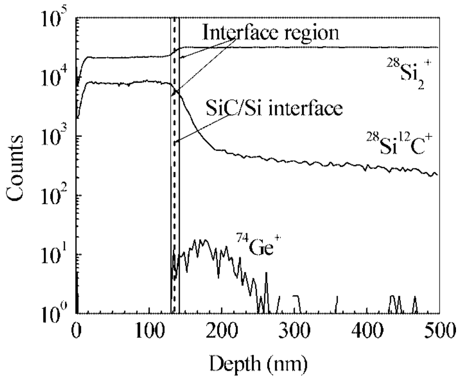

Figure 1. SIMS depth profile of the sample with 0.25 ML Ge pre-deposited at 325 °C.

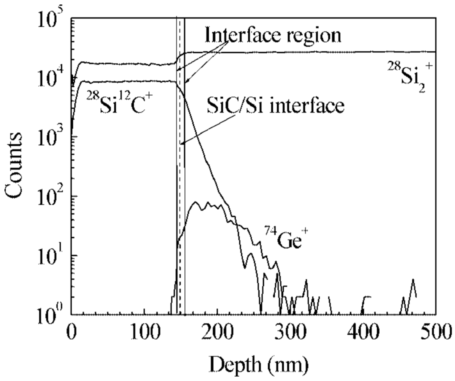

Figure 2. SIMS depth profile of the sample with 0.75 ML Ge pre-deposited at 325 °C.

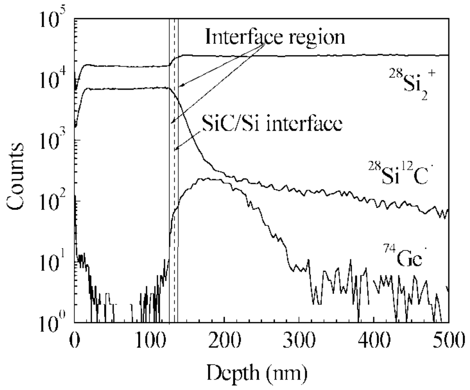

Figure 3. SIMS depth profile of the sample with 2 ML Ge pre-deposited at 325 °C.

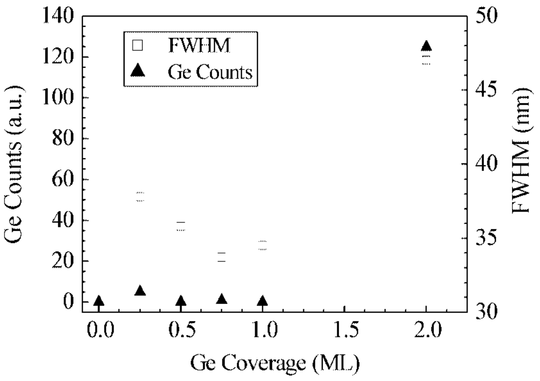

Figure 4. Ge surface concentration and FWHM of the Ge distribution versus Ge coverage.

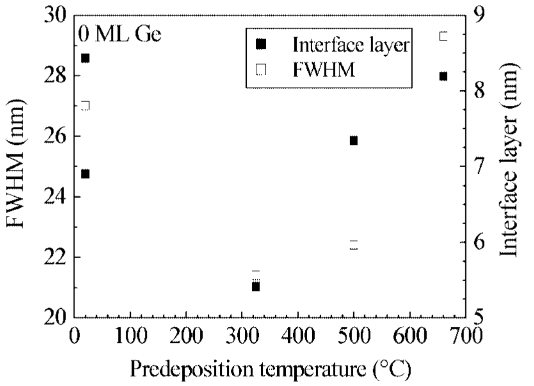

Figure 5. FWHM of the Ge distribution and interface width versus Ge pre-deposition temperature.

and at 2 ML. The height of the deep-reaching tail in the carbon distribution in terms of $^{28}Si^{12}C^+$ counts decreases with increasing Ge coverage. In the intermediate region only the steeper part of the carbon distribution is evident (Fig. 2). The steep part is confined within the region of the germanium distribution. The absence of the deep-reaching tail corresponds with narrower Ge distributions (Fig. 4) and smaller interface layers. In the region where only the steep part of the carbon distribution was observed the interface width was determined to be between 6 and 7 nm, whereas in the other cases the value was around 8 nm. As shown in Fig. 5, Ge deposition at elevated temperatures below 650 °C leads to further reduction of the interface width.

The observed features in the germanium and carbon distributions can be understood if the highly stressed nature of the SiC/Si heterostructure is taken into account. Under our conditions the SiC layer is normally under tensile stress whereas the silicon substrate is under compression.[4,5] Furthermore, the interface region contains a high concentration of dislocations and stacking faults. The density of the dislocations is around 10^{11} cm^{-2}.[6] Under these conditions independently of the precursors and growth techniques used in the beginning of the growth process a $Si_{1-x}C_x$ solid solution is formed.[7,8] If in this layer SiC nucleates then the compressive stress in the Si matrix pushes Si atoms from lattice sites into interstitial positions.[9] These interstitial atoms are diffusing onto the silicon surface and contributing in the early stages of the SiC formation to the further growth of the SiC nuclei. The Si atoms are incorporated into SiC leaving behind vacancies in the near-interface regions.[9] This process leads to interface roughening. If the vacancies concentration is high enough they can form nuclei of vacancies transforming into voids. Owing to the increasing stress in the SiC/Si heterostructure the driving force increases with increasing layer thickness leading to a continuous out-diffusion of Si if the diffusion coefficient in the SiC layer is high enough. The SiC layer peels off if an infinite void cluster in the silicon substrate is formed. On the other hand the voids contribute to stress reduction in the SiC/Si system.[10] The second stress reduction mechanism is the incorporation of carbon into Si lattice sites reducing the lattice constant and therefore the mismatch in the system. Because the solubility of carbon at lattice sites is limited, the excess carbon will occupy interstitial positions exhibiting a larger diffusion coefficient, which can be a cause for the deep tail in the carbon distribution.

If Ge is added at the early stages of the SiC formation and growth process, i.e. before and at the stage of the $Si_{1-x}C_x$ formation, it will be incorporated into the solid solution. As a result the lattice constants between the Si and the $Si_{1-x}C_x$ solid solution would be adjusted and the energy of the system will be lowered. Therefore, the formed $Si_{1-x-y}C_xGe_y$ layer contributes to the stress reduction in the SiC–$Si_{1-x}C_x$–Si system as shown in Ref. 11 in the case of epitaxial growth of $Si_{1-x-y}C_xGe_y$ solid solutions on Si and predicted for the SiC–Si system in Ref. 12. At the later stages the Ge may occupy the formed vacancies and defect sites in the near-interface region. Owing to the larger atomic radius of Ge and the stress it will be pushed out of the SiC lattices and will reside near the SiC/Si interface at the Si side. On the other hand, Ge is not able to form carbides.[13] For this reason it will not be incorporated into the SiC lattice with high concentrations. Furthermore, the several orders of magnitude lower diffusion coefficients of impurities in SiC compared to Si restricts the diffusion of Ge into SiC. So the relaxation of the initial Ge distribution into the Si substrate is more preferable leading to a diffusion of Ge into the silicon substrate. Owing to the stress reduction in the SiC/Si system by Ge incorporation[5,12] the driving force for the Si out-diffusion lowers and the Si vacancy formation at the SiC/Si interface is reduced. As a consequence the probability of the interface roughening is reduced and a sharper interface will be formed. This mechanism will be effective starting with a critical Ge coverage of around 0.25 ML. This can be deduced from the observed suppression of the Ge surface segregation if the pre-deposition coverage exceeds this value. The SE measurements also supported this conclusion. They revealed a substantial reduction of the interface width from 6.5 and 3.6 nm in the cases of 0 and 0.25 ML, respectively, to 0.5 nm at larger Ge coverages.

Furthermore, the effect of void formation reduction was observed by TEM studies (not shown here).[6] The stress reduction in the heteroepitaxial system may also be the cause of the carbon distribution confinement within the Ge segregation layer when a critical Ge content is reached (Fig. 2). Under our experimental conditions this effect was observed for Ge coverages above 0.5 ML and below 2 ML.

To understand the behaviour at 2 ML Ge it has to be taken into account that Ge pre-deposition leads to a decrease of the nucleation density and to an increase of the surface roughness from *rms* values between 0.7 and 1.7 nm for Ge coverages below 1 ML to *rms* values between 1 and 3 nm for Ge coverages equal to and above 1 ML Ge.[14,15] If this effect is too strong the subsequent epitaxial growth will be deteriorated and a high concentration of grain boundaries will be formed in the epitaxial layer. As a consequence strong grain boundary diffusion will occur leading to Ge surface segregation and Ge out-diffusion (Fig. 3).

CONCLUSION

Using SIMS the role of Ge incorporation into the SiC/Si heteroepitaxial system was studied. It was found that Ge, independently of the pre-deposited amount, remains near the SiC/Si interface on the silicon side at growth temperatures, which will normally lead to strong out-diffusion or diffusion of Ge into the Si substrate. The observed behaviour of Ge is caused by the specific stress and defect structure at the SiC/Si interface. The Ge pre-deposition prior to the carbonization of Si leads to an improvement of the interface structure in terms of interface sharpness and narrower Ge and C distributions if the Ge coverage is between 0.5 ML and 2 ML and if the Ge deposition is carried out at substrate temperatures between 300 and 600 °C.

Acknowledgements

The authors thank Volker Cimalla for the fruitful discussions and Thomas Stauden for the MBE operation.

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