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Transmission electron microscopy study of ultra-thin SiC layers obtained by rapid thermal carbonization of Si wafers

F. M. Morales[*, 1], **S. I. Molina**[1], **D. Araújo**[1], **V. Cimalla**[2], **J. Pezoldt**[2], **L. Barbadillo**[3], **M. J. Hernández**[3], and **J. Piqueras**[3]

[1] Departamento de Ciencia de los Materiales e Ingeniería Metalúrgica y Química Inorgánica, Universidad de Cádiz, Apdo. 40, Puerto Real, 11510-Cádiz, Spain
[2] TU Ilmenau, FG Nanotechnologie, Zentrum für Mikro- und Nanotechnologien, Postfach 100565, 98684 Ilmenau, Germany
[3] Laboratorio de Microelectrónica, Facultad de Ciencias, C-XI 100, Universidad Autónoma de Madrid, 28049 Cantoblanco, Madrid. Spain

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A structural multitechnique study of β-SiC/Si(111) and β-SiC/Si(100) wafers is reported in this paper. SiC thin layers have been developed in a Rapid Thermal Chemical Vapor Deposition (RTCVD) system by Si carbonization with propane. The study was carried out by High Resolution and Conventional Transmission Electron Microscopy (TEM), Selected Area Electron Diffraction (SAED), Spectroscopic Ellipsometry (SE), Fourier Transform Infra-Red Spectroscopy (FTIR) and Single Wave Length Multiple Angle (SWLMA) measurements. The thickness variations of the carbonized layer are determined along radial directions in both wafers by High Resolution Transmission Electron Microscopy (HRTEM). The latter are compared with average thickness determinations obtained by SE. The analyses confirm the existence of β-SiC layers with thicknesses of few nanometers in 3 inch SiC/Si wafers. Plan-view SAED evidences the existence of good structural quality and well aligned (111) and (001) β-SiC layers. Compositional and structural homogeneity indicates a self-limiting conversion mechanism of the Si surface into SiC. These are encouraging results in order to use the Si carbonization to grow stoichiometric crystalline III–N thin layers on Si. In fact, the obtained substrates in this work are actually used for a further GaN overgrowth.

Introduction Silicon carbide (SiC) is a wide band gap semiconductor and has been extensively considered for electronic devices operating at extreme conditions of high temperature, high frequency, high power, high radiation and chemically aggressive ambient [1]. The carbonization of Si allows the attainment of good quality β-SiC layers [2, 3]. These SiC/Si substrates are an ideal template for further SiC or III–N overgrowth [4]. The purpose of this work is to demonstrate the good quality, homogeneity and control of thickness in SiC layers by carbonizing Si(111) and (001) wafers of 3″ in diameter.

Experimental Single side polished (100) and (111)Si wafers were carbonized in an RTCVD system [2]. Wafer A ((100)Si p-type, 2–4 Ω cm) was carbonized by a rapid thermal process using a mixture of 0.15% propane in H_2 during 60 s with a final temperature of 1280 °C and a ramp rate of 50 K/s. Wafer B

* Corresponding author: e-mail: fmiguel.morales@uca.es, Phone: +34-956 016 335, Fax: +34-956 016 288

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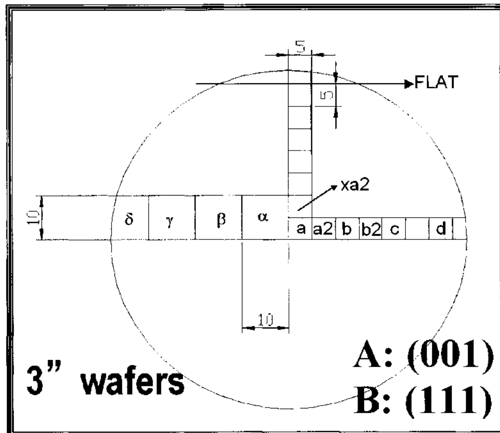


Fig. 1 Schematic view of assignment for specimens studied in each 3″ wafer. Samples were named starting with 0, if the wafer was (001) oriented (wafer A) and 1, if the wafer was (111) (wafer B). Samples α, β, γ, and δ (10 mm × 10 mm) were analyzed by FTIR and SE, while samples a, a2, b2, c, d, and ×a2 (5 mm × 5 mm) were prepared for XTEM and PVTEM.

((111) Si p-type, 1–20 Ω cm) was carbonized using the same mixture, time of carbonization and temperatures.

TEM, HREM, and SAED were the techniques used to study the inner crystalline structure of the samples, while FTIR, SE, and SWLMA measurements were used to check the thickness and the chemical nature of the layers in a more macroscopic way. Specimens were prepared for cross section TEM (XTEM) and plan view TEM (PVTEM), using mechanical thinning and Ar^+ milling at 4.5 kV in a Gatan Dual Ion Mill system. Conventional TEM was carried out in a JEOL JEM-1200EX electron microscope and a JEOL JEM-2000EX/THR was used for HRTEM. FTIR spectra in transmission mode were collected with a Bruker IFS-66V spectrometer in order to identify the vibrational bonds present in the sample. SE measurements were performed in an Uvisel Jobin-Yvon spectrometer between 1.5 eV and 4.5 eV.

Samples prepared for electron microscopy, SE and FTIR were catalogued following a criterion of distance from the center of the wafers. This assignment is shown in Fig. 1.

Results and discussion XTEM images of all samples show a well-defined homogeneous and continuous layer. The layer of wafer A (001) has an average measured thickness from HRTEM micrographs of about 2 nm.

In Fig. 2, TEM images of wafer A are shown. The thickness variations of the carbonized layer are determined along radial directions in the wafer. This layer has an average thickness measured from HRTEM images of 2.16 nm for zone 0a, 2.11 nm for zone 0b2, 1.99 nm for zone 0c and 1.81 nm for zone 0d. Voids around 15 nm of width and 3 nm of depth, are visualized below the carbonized layer of the wafers from high-magnification TEM images.

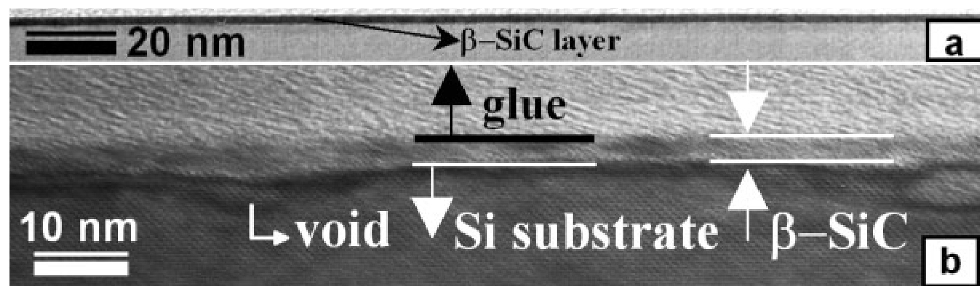
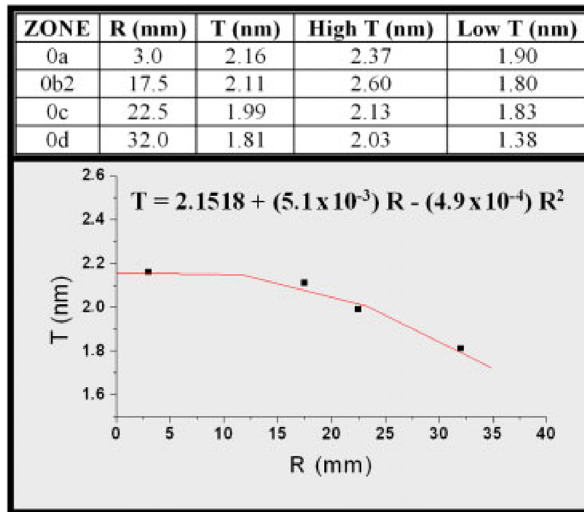


Fig. 2 XTEM images of sample preparations in wafer A. Figure 2a corresponds to a XTEM image for zone 0a, and Fig. 2b shows the aspect of the contrasted layer in HREM images for zones 0b2.



ZONE	R (mm)	T (nm)	High T (nm)	Low T (nm)
0a	3.0	2.16	2.37	1.90
0b2	17.5	2.11	2.60	1.80
0c	22.5	1.99	2.13	1.83
0d	32.0	1.81	2.03	1.38

Fig. 3 (online color at: www.interscience.wiley.com) T vs. R dependence. The table shows data of average, highest and lowest HREM measured thickness in samples 0a, 0b2, 0c, and 0d of wafer A. Although changes in thickness were measured, layers are mainly flat and continuous. The thickest parts of the layers often coincide with the upper limits of voids under the SiC layer, while the thinnest parts of the carbonized layer are placed far away from voids. The interface region of the converted wafers is rougher than the surface of the formed SiC layer.

The behavior of the layers average thickness T (nm) versus the radial distance to the wafer center R (mm) is deduced to fit a polynomial function having a flat maximum in the central region of the wafer by the expression: $T = 2.1518 + (5.1 \times 10^{-3})\,R - (4.9 \times 10^{-4})\,R^2$. For this system, light changes in the SiC thickness were previously proposed to be due to a non-homogeneous lamp-field, that affects the two-dimensional growth temperature across the wafer [2]. The graphic and the data used as well as the largest and shortest thickness measured in each sample are shown in Fig. 3. It is important to note, that HREM micrograph artifacts as for example that caused by Fresnel contrasts, the presence of amorphized zones or dark contrasts due to strain in the interface, can affect the thickness measurement accuracy. This accuracy is estimated in our case to be about ± 0.27 nm, that corresponds to the distance between Si(002) planes parallel of the (001)Si matrix used in our HREM study as reference.

In order to improve the thickness measurements, these results of cross section HRTEM analysis are compared with SE measurements made on similar areas and SWLMA measurements for larger areas. SWLMA at 632 nm allows to estimate an average thickness around 2.47 nm for the carbonized layer of wafer A. These measurements are carried out using a 3C–SiC/Si single layer model. On the other hand the SE technique allows to deduce the layer thickness and the composition adjusting the experimental curves to theoretical ones. SE measurements are less accurate but give us an idea of the SiC thickness tendency for bigger regions. A thickness of 3.1 nm and a composition of 91% of SiC plus 9% of crystalline Si (c-Si) is obtained in the region 0α of the carbonized substrate, 3.2 nm is obtained for zone 0β (91% SiC + 9% c-Si), 3.4 nm for zone 0γ (92% SiC + 8% c-Si) and 3.1 nm for zone 0δ (92% SiC + 8% c-Si). FTIR analysis for zones 0α, 0β, 0γ, and 0δ demonstrates the β-SiC nature of the over layer.

The XTEM micrograph of Fig. 4 shows a well-defined homogeneous and continuous SiC layer corresponding to region 1a of wafer B. This layer presents an average XTEM measured thickness of 3.12 nm although this value oscillates between 2.60 to 3.40 nm along the specimen. SWLMA at 632 nm allows to evaluate an average thickness of 3.14 nm for the carbonized layer, that corroborates XTEM results. The SE resulting average composition corresponds to 94% of SiC and 6% of crystalline Si. The SE deduced thickness is 3.7 nm for region 1α (95% SiC + 5% c-Si), 3.8 nm for region 1β (94% SiC + 6% c-Si),

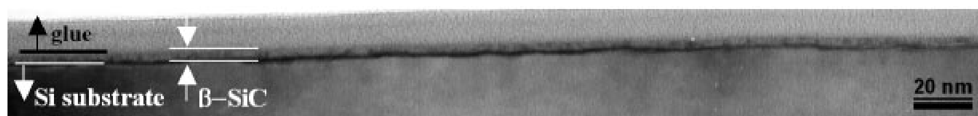


Fig. 4 XTEM micrograph of a sample obtained from wafer B in the zone catalogued as 1a.

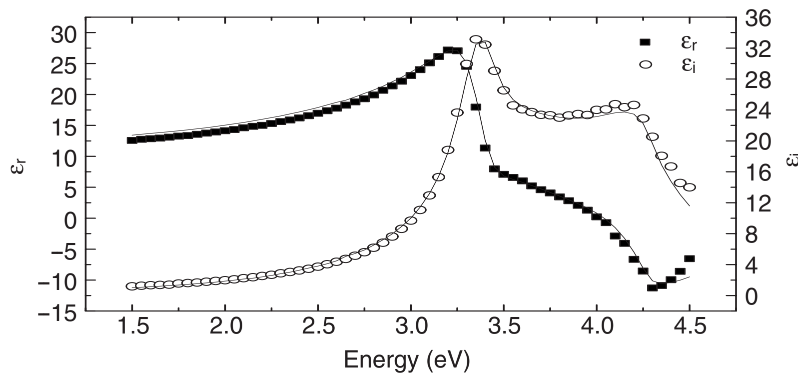


Fig. 5 SE spectrum (dots) and simulation (lines) of wafer B in place 1α. ε_r and ε_i represent the real and imaginary dielectric constants, respectively.

3.8 nm for region 1γ (93% SiC + 7% c-Si) and 3.5 nm for region 0δ (95% SiC + 5% c-Si). Figure 5 shows a SE spectrum of wafer B. FTIR analysis for these regions demonstrates β-SiC predominance again.

SAED patterns registered from both wafers in PVTEM orientation allow to certify a very well oriented single-crystalline β-SiC for all preparations. From these patterns, β-SiC(001)||Si(001) in plane misorientation is estimated to be around 3° and β-SiC(111)||Si(111) misorientation is measured to be about 2.5°.

Figure 6 shows a plan view SAED pattern registered along [001] of wafer A. The pattern of Fig. 6a shows a schematic assignment of all the spots observed on the same SAED pattern of Fig. 6b. The contrast of this pattern is inverted to allow an easier visualization of the information included in it. The most intense ordered spots (white spots) of Fig. 6a are due to the (001)Si substrate. Spots ordered in the same

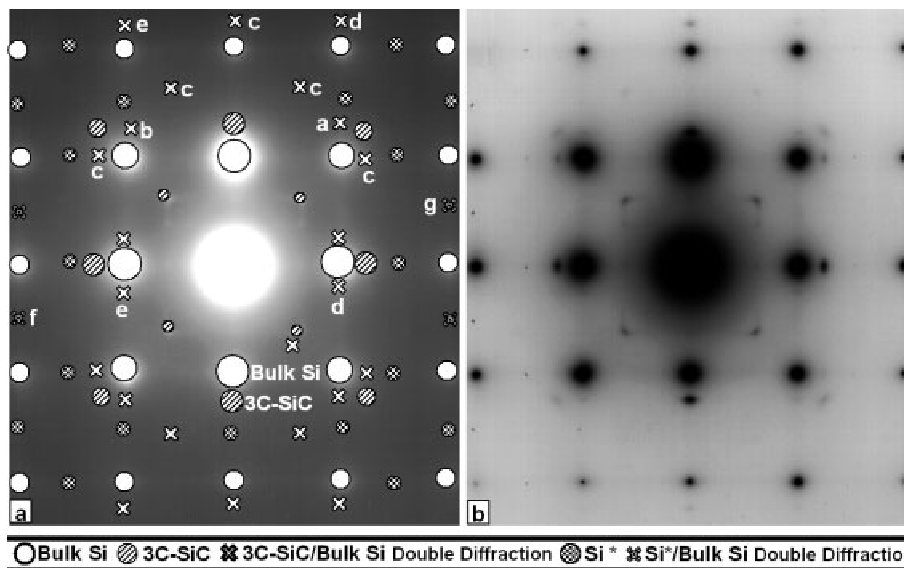


Fig. 6 SAED pattern registered from the SiC layer for PVTEM orientation in the [001] zone axis in the region defined as 0a2. Figure 6a represents the diffraction spots associated with the five main families of spots visualized in Fig. 6b. Few single-crystalline Si* grains are clearly observed to be orientated with the planes of the Si substrate.

arrangement but with different parameter (dashed spots) belong to the 3C–SiC diffraction, while the spots labeled as a, b, c and d (crosses) are originated by double diffraction between Si(001) and SiC(001). In this way, the "a" cross is originated by two successive diffractions: (i) 3C–SiC network, (ii) Si network with 2 2 0 incident orientation (i.e. situating a 220 Si spot in the transmitted beam). Similar double diffraction conditions centered on $2\ \bar{2}\ 0$, $\bar{2}\ 2\ 0$, 0 4 0 and $\bar{4}\ 0\ 0$ are indicated with "b", "c", "d", and "e", respectively. The spots situated between the Si main spots (dotted circles at distances of 1/2 of the distance between the Si spots) are indexed assuming the feasible presence of single-crystalline ⟨116⟩ Si* grains probably located inside the SiC layer, just on the interface or placed on the voids surface. The Si content is explained by assuming, that all outdiffusing Si promoted by a vacancy diffusion mechanism did not react with the incoming supplied C [5]. The other spots (dotted crosses f and g), are originated by double diffraction between both Si crystals: ⟨116⟩ Si* grain and the bulk [001] Si. For example, spots like "f" are originated if the transmitted beam of the Si* pattern is situated over the $\bar{4}\ 0\ 0$ diffracted spot of the bulk Si pattern. We have to take into account, that this third type of diffraction is evidenced only for SAED patterns registered at long times. This means, that these ⟨116⟩ Si* grains are not abundant. Spots indexed as 3C−SiC do not have a perfect circle shape, but have a slightly elongated shape along an arc of few degrees. These arcs result from the misorientation of β-SiC grains in a mosaic structure.

Figure 7 shows a planar view SAED pattern registered from the (111)SiC layer along the [111] zone axis and in the area defined as 1a2. The contrast of this pattern is inverted to allow an easier visualization of the information included in it.

The most intense ordered spots in the pattern (circles in gray) are originated by the (111)Si substrate. The spots ordered in the same radial direction (dotted circles) are caused by (111) 3C–SiC diffraction, while the spots originated by the double diffraction between Si(111) and SiC(111) are located around the Si spots at the same distances than the SiC ones (crosses). Spots indexed as 3C–SiC have a very slightly elongated shape. A small contribution of relaxed hexagonal SiC (dashed circles) is detected in these SAED patterns recorded for long exposure times. The assignation of 2H, 4H, 6H, and 8H phases to

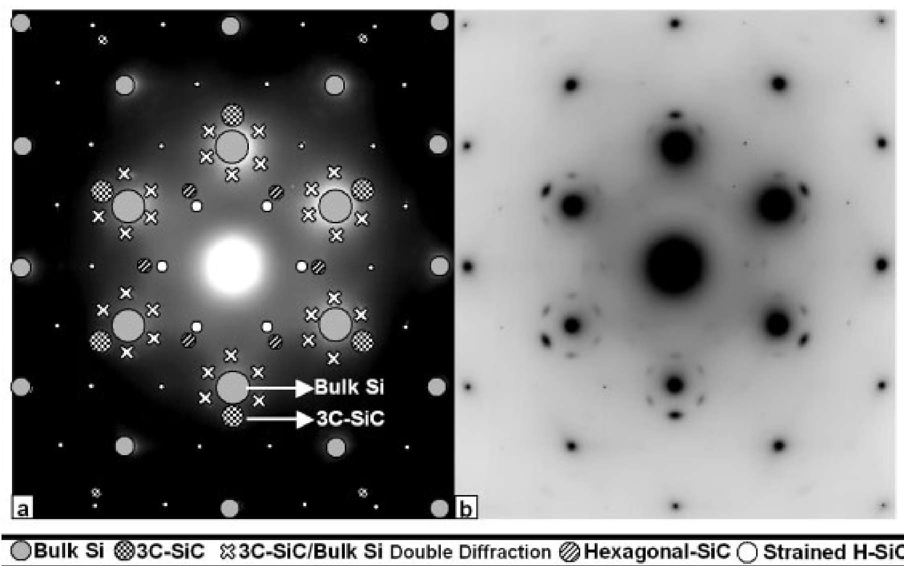


Fig. 7 SAED pattern for PVTEM preparation of wafer B registered along the [111] zone axis. Figure 7a represents the diffraction spots associated with families of spots visualized in Fig. 7b. The inset in Fig. 7b is a detail of contrasted hexagonal SiC dots. Double diffraction and a small amount of single-crystalline hexagonal strained and relaxed SiC grains are detected.

these hexagonal SiC spots is acceptable if dynamic conditions are taken into account. Anyway, the small thickness of the carbonized layer and the aspect of SAED pattern for kinematical conditions make favorable (after comparison of experimental and simulated SAED patterns), the presence of 2H and/or 4H polytypes. On the other hand, spots situated between the main spots (circles in white at distances of 1/3 of the distance between the origin and the {224} Si spots) can only be indexed assuming the existence of very strained thin (few monolayers) hexagonal [001] crystals deposited on the Si substrate (e.g. on the void surface). Similar experiments and thermodynamic considerations confirm that the existence of two analogous HCP and FCC polymorphs is possible in SiC [3, 5–7]. Carbon rich conditions, spiral growth or grain structures could promote the hexagonal presence. Stacking faults due to stress and grain boundary defects are introduced due to grains of the mosaic structure. The consequent relaxation by plastic deformation produces a change in the stacking sequence from cubic to hexagonal around the stacking fault. We have to note again, that this hexagonal SiC diffraction is evidenced only for SAED patterns registered at long times; that means that H–SiC grains are not abundant. Other explanation of these spots would be the forbidden {4/3 2/3 2/3} type reflections of Si, appearing when the density of the planar defects (twins and stacking faults) parallel to the (111) plane is very high, but we did not detect such planar defects.

Conclusion Carbonization using propane as C precursor by a rapid thermal process leads to the formation of ultra-thin β-SiC(001)//Si(001) and β-SiC(111)//Si(111) structures. The SiC exhibits well-orientated nano-layers, good crystalline quality and homogeneity as a consequence of a self-limiting conversion mechanism of the Si surface into SiC. By this reason, the heterostructures show few voids (in their first stages of formation). The interface region of the converted wafers is rougher than the surface of the formed SiC layer.

These 3″ SiC/Si wafers exhibit an homogeneous thickness and are flat and continuous all over the specimen surface. These parameters are very important in order to integrate the SiC/Si wafers in opto/microelectronic device technologies, being ideal as substrates for further SiC or III–N re-growth, i.e. using the carbonized layer as buffer.

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